CLAIMS

What is claimed is:

1. A signal line termination circuit, comprising:

a software controller for providing a control signal for selectively causing a signal line to be pulled to a voltage level;

a mechanism for permitting the setting of a mode for the signal line, the mechanism receiving the control signal from the software controller and providing an enablement signal; and

a switch for controlling power to the signal line through the enablement signal, the switch being controllable by the mechanism by the transmitted control signal.

2. The signal line termination circuit of Claim 1, further comprising a bus terminator that receives the output signal of the switch.

3. The signal line termination circuit of Claim 2, wherein the mechanism is controlled by a manual setting of the mechanism by an operator.

4. The signal line termination circuit of Claim 3, wherein the mechanism is a three jumper pin unit.

5. The signal line termination circuit of Claim 3, wherein the mechanism is a three position manual switch.

6. The signal line termination circuit of Claim 1, wherein the mechanism is controlled by an automatic setting of the mechanism.

7. The signal line termination circuit of Claim 6, wherein the automatic setting is

performed by operation of the software controller.

8. The signal line termination circuit of Claim 7, wherein the software controller is a complex programmable logic device.

9. The signal line termination circuit of Claim 7, wherein the software controller is a field programmable gate array.

10. The signal line termination circuit of Claim 1, wherein the mechanism is a three point mechanism having a first point, a second point, and a third point.

11. The signal line termination circuit of Claim 10, wherein the control signal of the software controller is directly electrically connected to the first point and is applied to the third point through a resistor so that the resistor electrically connects the first and third points.

12. The signal line termination circuit of Claim 11, wherein the third point is directly electrically connected to circuit ground.

13. The signal line termination circuit of Claim 12, wherein the second point is directly electrically connected to a control terminal of the switch.

14. The signal line termination circuit of Claim 13, wherein the switch, in addition to the control terminal, includes a power side terminal and a ground side terminal.

15. The signal line termination circuit of Claim 14, wherein the control terminal is electrically connected to power through a first passive element and the power side terminal is electrically connected to power through a second passive element.

16. The signal line termination circuit of Claim 15, wherein the power side terminal of the switch is feedback to the software controller.

17. The signal line termination circuit of Claim 16, wherein the software controller is communicatively coupled to a host processor.

18. The signal line termination circuit of Claim 17, wherein the first and second passive elements are resistors.

19. A method for setting a bus signal line termination state, comprising:

setting a mode of operation of bus signal line termination from multiple bus signal line termination states;

determining if the bus signal line is under software control;

if it is determined that the bus signal line is under software control, setting the enablement state of the bus signal line under software control.

20. The method of Claim 19, further comprising, if the bus signal line is not under software control, determining a state of the bus signal line termination.

21. The method of Claim 19, further comprising switching between the multiple bus signal line termination states.

22. The method of Claim 19, wherein setting a mode of operation is accomplished manually.

23. The method of Claim 22, wherein the manual setting is through jumper wires.

24. The method of Claim 22, wherein the manual setting is through manual setting of a switch.

25. The method of Claim 19, wherein setting a mode of operation is accomplished automatically.

26. A method of controlling a termination state of a signal line, comprising:

loading a sense register with a current state of a termination sense signal; and

if a reset signal is not active, then determining if a software select mode has been enabled.

27. The method of Claim 26, further comprising, if the software select mode has not been enabled, reporting that software does not control termination.

28. The method of Claim 27, further comprising determining a logic level of a disconnect status signal.

29. The method of Claim 28, further comprising, if the logic level of the disconnect status signal is a logic high, reporting that termination is hardware disabled and set at a logic high level.

30. The method of Claim 28, further comprising, if the logic level of the disconnect status signal is a logic low, reporting that termination is hardware enabled and set at a logic low.

31. The method of Claim 26, further comprising, if the software select mode has been enabled, enabling or disabling termination of the bus signal line.

32. A circuit for selectively enabling software control of the termination for a bus signal line, comprising:

a means for providing software control of a bus signal line termination;

a means for setting a mode of enablement for a bus signal line termination in which the means for setting a mode of enablement receives a signal from the means for providing software control; and

a means for switching between a pull up mode and a pull down mode on the bus signal line in accordance with a signal provided by the means for setting a mode.

33. The circuit of Claim 32, further comprising a means for terminating a bus signal coupled to the means for switching.

34. The circuit of Claim 33, wherein the bus signal is a Small Computer System Interface (SCSI) bus signal.

35. The circuit of Claim 33, wherein the bus signal is a Peripheral Component Interconnect (PCI) bus signal.